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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 10/723,347      | 11/25/2003  | Zohar Bogin          | P17517              | 8242             |

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EXAMINER

MARTINEZ, DAVID E

ART UNIT PAPER NUMBER

2181

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                   |              |  |
|------------------------------|-------------------|--------------|--|
| <b>Office Action Summary</b> | Application No.   | Applicant(s) |  |
|                              | 10/723,347        | BOGIN ET AL. |  |
|                              | Examiner          | Art Unit     |  |
|                              | David E. Martinez | 2181         |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 02 May 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

*Fritz Fleming*  
**FRITZ FLEMING**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**  
*7/19/2006*

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1/17/06</u>   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Objections***

Claim 1 is objected to because of the following informalities: There seems to be a typo in line 1, the term "In a controller of a computing device, computing device comprising..." appears to be missing a "the" after the comma. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 6, it is not understood what is being determined. Is the Applicant trying to determine if to update or not, a value in system memory? It appears that perhaps the claim is trying to recite that the value is constantly being updated and no determination is ever being done. If the value is constantly automatically being updated when a transfer takes place, there is no determination taking place. Or is the claim trying to recite "determining the value to update"?

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3-7, 9-13, 16, 19, 20, 25, 27 and 28, are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason).

1. With regards to claim 1, Hoang teaches in a controller [fig 1 element 20, details shown in fig 2] of a computing device [fig 1 system 10, column 2 lines 19-38], computing device comprising a system memory [fig 1 element 16] and a codec [fig 1 element 32], a method comprising

reading data from a buffer [fig 1 element 16] of the system memory [fig 1 element 16] via a first interface of the controller [fig 2 element 22, column 3 lines 28-39],

transferring the data to the codec via a second interface of the controller [fig 2 element 26, column 3 lines 28-39],

tracking a position in the buffer from which the controller has read the data [fig 2 element 78, column 3 lines 29-32, column 5 lines 45-49],

Hoang teaches storing a value in an register to indicate the position in the buffer [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 29-32,]. Hoang teaches all of the above limitations except for writing a value to the system memory via the first interface to indicate the position in the buffer. However, Mason teaches a controller that writes values to the system memory via an interface instead of storing them in internal registers to reduce the amount of internal hardware in the controller and improve efficiency and overall performance [column 2 line 48 to column 3 line 3, column 14 lines 19-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Hoang and Mason to write a value to the system memory via the first interface to indicate the position in the buffer to reduce the amount of internal hardware in the controller and improve efficiency and overall performance.

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2. With regards to claim 3, Hoang teaches the method of claim 1 further comprising tracking progress of transferring the data to the codec via the second interface [column 3 lines 29-50].
3. With regards to claim 4, Hoang teaches the method of claim 1 wherein reading the data from the buffer comprises reading the data per a buffer descriptor list that defines the buffer [fig 2 elements 50, 52, 70, 72].
4. With regards to claim 5, Hoang teaches the method of claim 4 wherein reading the data from the buffer further comprises returning to a start of the buffer in response to reaching an end of the buffer [column 4 lines 24-35].
5. With regards to claim 6, Hoang teaches the method of claim 1 further comprises, prior to writing the value to system memory, determining to update the value in the system memory based upon the data transferred via the second interface [column 4 lines 29-32].
6. With regards to claim 7, Hoang teaches in a controller [fig 1 element 20, details shown in fig 2] of a computing device [fig 1 system 10, column 2 lines 19-38], the computing device comprising a system memory [fig 1 element 16] and a codec [fig 1 element 32], a method comprising  
  
receiving data from the codec [fig 1 element 32] via a first interface of the controller [figs 1, 2 element 28, column 2 lines 39-49],  
  
writing the data to a buffer of the system memory via a second interface of the controller [figs 1 element 16, column 2 lines 39-49],  
  
tracking a position in the buffer to which the controller has written the data [column 3 lines 29-32],  
  
Hoang teaches storing a value in an register to indicate the position in the buffer [fig 2 elements 58 and 78, column 3 lines 21-24, column 4 lines 29-32,]. Hoang teaches all of the

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above limitations except for writing a value to the system memory via the second interface to indicate the position in the buffer. However, Mason teaches a controller that writes values to the system memory via an interface instead of storing them in internal registers to reduce the amount of internal hardware in the controller and improve efficiency and overall performance [column 2 line 48 to column 3 line 3, column 14 lines 19-31].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Hoang and Mason to write a value to the system memory via the second interface to indicate the position in the buffer to reduce the amount of internal hardware in the controller and improve efficiency and overall performance.

7. With regards to claim 9, it is of the same scope as claim 3 above and thus is rejected under the same rationale.

8. With regards to claim 10, it is of the same scope as claim 4 above and thus is rejected under the same rationale.

9. With regards to claim 11, it is of the same scope as claim 5 above and thus is rejected under the same rationale.

10. With regards to claim 12, it is of the same scope as claim 6 above and thus is rejected under the same rationale.

11. With regards to claim 13, Hoang teaches a system [fig 1] comprising  
a processor [fig 1 element 12],

a system memory [fig 1 element 16] comprising a buffer [fig 1 element 16] and a buffer position, that indicates a position in the buffer [the combination of Hoang and Mason for the same reasons as those set forth under the claim 1 and 7 rejection above],

an audio controller [fig 1 element 20] coupled to the system memory [fig 1 element 16] via a first bus [fig 1 element 11], and

a codec [fig 1 element 32] coupled the audio controller [fig 1 element 20] via a second bus [fig 1 element 20 has the buffers and codec interfaces connected over a bus to element 32], wherein

the audio controller [fig 1 element 20] transfers data between the buffer [fig 1 element 16] and the codec [fig 1 element 32] via the first bus [fig 1 element 11] and the second bus [fig 1 element 20 has the buffers and codec interfaces connected over a bus to element 32] and updates the buffer position via the first bus to indicate a position in the buffer associated with the audio controller transferring between the buffer and the audio controller [column 4 lines 24-35].

12. With regards to claim 16, it is of the same scope as claim 4 above and thus is rejected under the same rationale. Furthermore, it would have been obvious to store the descriptor list in system memory for the same reasons set forth under the claim 1 rejection above taught by the combination of Hoang and Mason.

13. With regards to claim 19, it is of the same scope as the combination of claims 1 and 7 above and thus is rejected under the same rationale.

14. With regards to claim 20, it is of the same scope as claims 1 and 4 above, and thus is rejected under the same rationale. Furthermore, Hoang teaches the buffer descriptor list is included in the dma controller [fig 1 and 2 element 20] rather than inside the system memory. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the buffer descriptor list in the system memory for the same reasons as those set forth in the claim 1 rejection above.

15. With regards to claim 25, it is of the same scope as claim 13 above and thus is rejected under the same rationale.

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16. With regards to claim 27, Hoang teaches the machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

allocating the buffer in the system memory [allocating takes place when the controller (fig 1 element 20) is instructed to storing data in the system memory] and storing a buffer descriptor list in the system memory [same scope as a combination of claim 16 and 1 above thus rejected under the same rationale], and

configuring the audio controller to transfer the data per the buffer descriptor list [same scope as claim 16 and 1 above].

17. With regards to claim 28, Hoang teaches the machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

allocating a position in buffer structure in the system memory [this is done when storing data in the memory buffer, the particular position must be allocated in order to be filled, ], and

configuring to update the position in buffer structure with the buffer position [same scope as in claim 1 above].

Claims 2, 8, 14, 17, 18, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason) further in view of Applicant's Admitted Prior Art (hereinafter AAPA).

18. With regards to claim 2, Hoang teaches receiving the data via the first interface [fig 2 element 22, column 3 lines 28-39], but the combination of Hoang and Mason are silent as to wherein reading comprises isochronously receiving the data via the first interface. However, AAPA teaches using isochronous data transfers for the benefit of helping multimedia



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applications such as audio and video applications achieve high quality results [page 1, paragraph 1].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and AAPA to isochronously receive the data via the first interface for the benefit of helping multimedia applications such as audio and video applications achieve high quality results.

19. With regards to claim 8, it is of the same scope as claim 2 above and thus is rejected under the same rationale.

20. With regards to claim 14, it is of the same scope as claim 2 above and thus is rejected under the same rationale.

21. With regards to claim 17, it is of the same scope as the combination of claims 1 and 2 above and thus is rejected under the same rationale.

22. With regards to claim 18, it is of the same scope as the combination of claims 7 and 2 above and thus is rejected under the same rationale.

23. With regards to claim 23, it is of the same scope as claim 2 above, when transfers are directed to writing data isochronously, and thus is rejected under the same rationale.

24. With regards to claim 24, it is of the same scope as claim 2 above, when transfers are directed to reading data isochronously, and thus is rejected under the same rationale.

Claims 15, 21, 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,792,481 to Hoang et al. (hereinafter Hoang) in view of US Patent No. 6,418,489 to Mason et al. (hereinafter Mason) further in view of US Patent No. 6,693,753 to Su et al. (hereinafter Su)

25. With regards to claim 15, Hoang teaches the system of claim 13 wherein the audio controller [fig 1 element 20] transfers the data across a link of the first bus [fig 1 element 11] but

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is silent as to updating a link position counter of the audio controller based upon the data transferred across the link. However, Su teaches using a link position counter in an interface between two communicating devices for the benefit of tracking the progress of the data transfer [column 7 lines 4-22].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Hoang, Mason and Su to update a link position counter of the audio controller based on the data transferred across the link for the benefit of tracking the progress of the data transfer.

26. With regards to claim 21, it is of the same scope as claim 15 above and thus is rejected under the same rationale.

27. With regards to claim 22, it is of the same scope as claim 15 above and thus is rejected under the same rationale.

28. With regards to claim 26, it is of the same scope as claim 15 above and thus is rejected under the same rationale.

### ***Response to Arguments***

Applicant's arguments filed 5/2/06 have been fully considered but they are not persuasive.

With regards to Applicant's arguments directed to claim 1 (remarks pages 15 to 18), Examiner respectfully disagrees. The Examiner only relies on the Mason reference for "writing a value to the system memory via the first interface to indicate the position in the buffer" and not for "reading data from a buffer of the system memory via a first interface" which is disclosed by the Hoang reference. In column 2, lines 40-60, Mason teaches the use of memory (system memory line 41) for storing context information (lines 52-60 storing in a first, second and third memory location).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it was shown by the references that the combination of Hoang and Mason would lead to reducing the amount of internal hardware in the controller improving efficiency and overall performance [Mason column 2 line 48 to column 3 line 3, column 14 lines 19-31]. Not only is that benefit taught by Mason, but also one of ordinary skill in the art at the time of the invention would have also seen that the Mason reference would have improved the Hoang DMA controller, by using context switching between tasks (processes), allowing the DMA controller to also handle more than one process at the same time and thus increasing overall throughput in the system. Contrary to the Applicant's analysis, the differences between the DMA controllers taught by Mason and Hoang does not impede the two from being combined. The differences are due to the different features that each DMA controller has and the modifying the DMA controller of Hoang would only provide the benefits of those particular features being borrowed from Mason.

With regards to dependent claims 3-7, 9-13, 16, 19, 20, 25, 27 and 28, they stand rejected for the same reasons as those set forth above.

With regards to the 103 rejections directed to claims 2, 8, 14, 17, 18, 23, 24, and 15, 21, 22 and 26, they stand rejected for the same reasons as those set forth above.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

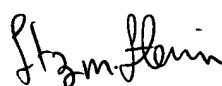
Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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7/19/2006